FORM PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. IMEC279.001AUS	APPLICATION NO. 10/603,426
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		APPLICANT Van Houdt, et al.	
(USE SEVERAL SHEETS IF NECESSARY)		FILING DATE June 24, 2003	GROUP 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
AL	1	4,794,565	12/27/88	Wu, et al.			
	2	5,278,439	01/11/94	Ma, et al.			
	3	5,280,446	01/18/94	Ma, et al.			
	4	5,284,784	02/08/94	Manley			
	5	5,338,952	08/16/94	Yamauchi			
	6	5,394,360	02/28/95	Fukumoto			
	7	5,538,811	12/10/96	Van Houdt, et al.			
	8	5,841,697	11/24/98	Van Houdt, et al.			
	9	6,044,015	03/28/00	Van Houdt, et al.			
	10	6,366,500 B1	04/02/02	Ogura, et al.			
	11	6,580,120 B1	06/17/03	Haspeslagh			
AL	12	2002/0005545 A1	01/17/02	Widdershoven, et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
AL	13	EP 1 096 572 A1	05/02/01	EUROPE				

EXAMINER INITIAL		OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
AL	14	Esquivel, et al., "High density contactless, self aligned EPROM cell array technology", IEDM Tech. Dig., pp. 592-595, (1986).
	15	Hayashi, et al., "Twin MONOS cell with dual control gates", IEEE, presented at the 2000 Symposium on VLSI Technology Digest of Technical Papers, pp. 122-123, (2000).
	16	*Microlithography, Science and Technology*, Sheats, et al., Eds., Marcel Dekker, Inc., New York, New York, pp. 515-565 and 615-644, (1998).
	17	Miyawaki, et al., "A new erasing and row decoding scheme for low supply voltage operation 16-Mb/64-Mb flash memories", IEEE Journal of Solid-State Circuits, vol. 27, no. 4, pp. 583-588, (April 1992).
	18	Tanaka, et al., "A quick intelligent page-programming architecture and a shielded bitline sensing method for 3V-only NAND flash memory", IEEE Journal of Solid-State Circuits, vol. 29, no. 11, pp. 1366-1373, (November 1994).
AL	19	Van Houdt, et al., "A 5-volt-only fast-programming flash EEPROM cell with a double polysilicon split-gate structure", presented at the 11th IEEE Non-volatile Semiconductor Memory Workshop, (February 1991).

EXAMINER	Andrei Mirpuri	DATE CONSIDERED	07/19/04

*EXAMINER: INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED. INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. IMEC279.001AUS	APPLICATION NO. 10/603,428
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	APPLICANT Van Houdt, et al.	
(USE SEVERAL SHEETS IF NECESSARY)	FILING DATE June 24, 2003	GROUP 2818

EXAMINER INITIAL		OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
AH	20	Van Houdt, et al., "Analysis of the enhanced hot-electron injection in split-gate transistors useful for EEPROM applications, IEEE Transactions on Electron Devices, vol. 39, no. 5, pp. 1150-1156, (May 1992).
	21	Van Houdt, et al., "HIMOS-A high efficiency flash E2PROM cell for embedded memory applications", IEEE Transactions on Electron Devices, vol. 40, no. 12, pp. 2255-2263, (December 1993).
AH	22	Yamauchi, et al., "A 5V-only virtual ground flash cell with an auxilliary gate for high density and high speed application", IEDM Tech. Dig., p. 319-322, (1991).

S:\DOCS\MMA\MMA-7547.DOC/cfg/091703

EXAMINER	DATE CONSIDERED 07/19/04

*EXAMINER: INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED, INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.